UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/374,502	08/13/99	MA	Q 42390.P6623

MM91/0917

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EXAMINER	
FENTY, J	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 09/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/374,502	Applicant(s) MA ET AL.	
	Examiner Jesse A Fenty	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24, 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1, 2, 5, 8, 15, 18, 20, 23 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong et al. (U.S. Patent No. 6,083,797).

In re claim 1, Wong (Fig. 2D) discloses a semiconductor device, comprising:

An active area formed in a semiconductor substrate; and

An isolation structure (12) comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area.

The limitation, "wherein at least ... is adapted to ... area" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 2, Wong discloses the device of claim 1, wherein said active area further comprises an NMOS transistor.

In re claim 5, Wong discloses the device of claim 2, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

In re claim 8, Wong discloses the device of claim 1, wherein said active area further comprises an PMOS transistor.

In re claims 15 and 20, Wong discloses the device of claim 8, wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the PMOS device components having a depth wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench parallel and perpendicular to a channel current direction of the PMOS device having a depth such that an aspect ration of said trench portion depth to said active area width is greater than about 0.5.

In re claim 18, Wong discloses the device of claim 15, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the PMOS device components.

In re claim 23, Wong discloses the device of claim 20, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the PMOS device components.

In re claim 31, Wong (Fig. 2D) discloses a semiconductor device, comprising:

An active area formed in a semiconductor substrate; and

A stress modifying isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. as applied to claim 2 above, and further in view of Lur (U.S. Patent No. 5,395,790).

In re claims 3, 4, 6 and 7, Wong discloses the devices of claims 2 and 5 respectively, but does not expressly disclose the isolation structure comprising a low-modulus dielectric. Lur discloses an isolation structure using a low-modulus dielectric (polyimide, 29). It would have been obvious to one skilled in the art at the time of the invention to substitute a polyimide dielectric as taught by Lur for the device of Wong for the purpose, for example, solving the problems of crystalline defects or degraded characteristics of devices (Lur; Abstract) which may occur due to lack of stress-reducing support structures.

In re claims 9, 11, 13 and 14, Wong discloses the device of claim 8, but does not expressly disclose the isolation structure comprising a low-modulus dielectric. Lur discloses an

isolation structure using a low-modulus dielectric (polyimide, 29). It would have been obvious to one skilled in the art at the time of the invention to substitute a polyimide dielectric as taught by Lur for the device of Wong for the purpose, for example, solving the problems of crystalline defects or degraded characteristics of devices (Lur; Abstract) which may occur due to lack of stress-reducing support structures. The dielectric material is disposed in the trench both parallel and perpendicular to the channel current direction.

In re claim10, Wong in view of Lur discloses the device of claim 9, wherein said isolation structure comprises a high-modulus, dielectric material (Wong, line 47) disposed within said at least a portion of said trench parallel to a channel current direction of the PMOS device components.

In re claim 12, Wong in view of Lur discloses the device of claim 11, wherein said isolation structure comprises a high-modulus, dielectric material (Wong, line 47) disposed within said at least a portion of said trench parallel to the channel current direction of the PMOS device components.

In re claims 16, 17, 19, 21, 22 and 24, Wong discloses the devices of claims 15 and 20 repsectively, but does not expressly disclose the isolation structure comprising a low-modulus dielectric or tensile-stress inducing dielectric material. Lur discloses an isolation structure using a low-modulus dielectric (polyimide, 29). It would have been obvious to one skilled in the art at the time of the invention to substitute a polyimide dielectric as taught by Lur for the device of Wong for the purpose, for example, solving the problems of crystalline defects or degraded characteristics of devices (Lur; Abstract) which may occur due to lack of stress-reducing support

structures. The dielectric material is disposed in the trench both parallel and perpendicular to the channel current direction.

Response to Arguments

5. Applicant's arguments filed 06/20/01 have been fully considered but they are not persuasive.

First of all, Examiner thanks Applicant for pointing to the specific sections of the text which define the terms "low-modulus", "high-modulus" and "aspect-ratio"; giving the Examiner a refresher as to the claimed novelty of the invention. By those means the 112, 2nd paragraph rejections are vacated.

In response to the art rejection (Wong), applicant argues the "intended use" statement given by the Examiner in the 1st Office Action. This statement is sustained in the current rejection and also applies to new claim 31, although not mentioned explicitly. The language of claims 1 and 31, are written very broadly in terms of structural limitations, and it is the job of the examiner to interpret claims in their broadest scope. Although applicant claims (claim 1) that "at least a portion of said isolation structure is adapted to modify stresses incurred on said active area," the absence of any specific material or further limitation does not distinguish this claimed structure over the device of Wong. It can be interpreted that though the isolation dielectrics of Wong are considered, "high modulus," they still will have an effect on the stresses of the silicon substrate, which is what the claims imply.

In response to the subsequent arguments regarding "low modulus" and "low-tensile strength" dielectric materials, the new rejection above is submitted to address these claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on M-F 8-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A Fenty
Examiner
Art Unit 2815

JAF
September 10, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800